WHAT IS CLAIMED IS:

1. A channel architecture for use in automatic test equipment, the channel architecture comprising:

pattern generation circuitry;

timing circuitry responsive to the pattern generation circuitry to generate timing signals;

formatting circuitry coupled to the output of the timing circuitry to generate pulse waveforms; and

pin electronics circuitry responsive to the formatting circuitry for interfacing the automatic test equipment to a device-under-test, wherein the pattern generation circuitry, the timing circuitry, the formatting circuitry and the pin electronics circuitry are formed on the same integrated circuit.

2. A channel architecture according to claim 1 wherein the integrated circuit is formed by a silicon-on-insulator process.

3. A channel architecture according to claim 1 wherein the pattern generation circuitry, the timing circuitry and the formatting circuitry comprise low voltage digital circuits operating at voltage levels no greater than one volt.

4. A channel architecture according to claim 1 wherein the pin electronics circuitry comprises high-voltage analog circuits operating at voltages higher than one volt.

5. Automatic test equipment for testing semiconductor devices, the automatic test equipment comprising:

a controller; and

a testhead, the testhead adapted for housing a plurality of channel cards, each channel card comprising a plurality of integrated circuit chips, each chip comprising

pattern generation circuitry,

timing circuitry responsive to the pattern generation circuitry to generate timing signals;

formatting circuitry coupled to the output of the timing circuitry to generate pulse waveforms, and

pin electronics circuitry responsive to the formatting circuitry for interfacing the automatic test equipment to a device-under-test.

6. Automatic test equipment according to claim 5 wherein the integrated circuit is formed by a silicon-on-insulator process.

7. Automatic test equipment according to claim 5 wherein the pattern generation circuitry, the timing circuitry and the formatting circuitry comprise low voltage digital circuits operating at voltage levels no greater than one volt.

8. Automatic test equipment according to claim 5 wherein the pin electronics circuitry comprises high-voltage analog circuits operating at voltages higher than one volt.

9. A method of manufacturing a semiconductor device, the method comprising the steps:

selecting automatic test equipment comprising a controller and a testhead, the testhead adapted for housing a plurality of channel cards, each channel card comprising a plurality of integrated circuit chips, each chip comprising

pattern generation circuitry,

timing circuitry responsive to the pattern generation circuitry to generate timing signals;

formatting circuitry coupled to the output of the timing circuitry to generate pulse waveforms, and

pin electronics circuitry responsive to the formatting circuitry for interfacing the automatic test equipment to a device-under-test; and

testing the semiconductor device with the selected automatic test equipment.

10. A method of manufacturing a semiconductor device according to claim 9 wherein each chip is formed by a silicon-on-insulator process.